Per Vices Corporation

TECHNICAL DATASHEET

Per Vices Corporation
High Performance Software Defined for Low Latency Systems

TECHNICAL SPECIFICATIONS	10MHz	2800MHz	18000MHz
Dynamic range (dB)	>70	64	60
Typical Rx noise figure (dB) (see Note 1)	1.2	1.4	2.5
Max Tx output power (dBm) (see Note 1)	15	15	10
Latency (see Note 6)	<0.8c		
Min Rx demod SNR (see Note 5)	>10dB		
Error correction (FEC)	Yes		
Frequency tuning range	100 kHz to 18 GHz		
Tuning time between different frequencies (see Note 2)	2ms		
Fast tuning time between frequencies (see Note 2)	40us		
Storage temperature	0-40 C		
Operating temperature	5-40 C		
Number of FPGA logic elements	350k (Crimson) / 2800k (Cyan)		
Peak floating-point performance (# of TFLOPS)	9.2 (Cyan)		
API documentation	Yes		
Antenna interface (see Note 1)	50Ω SMA		
Data interface (see Note 1)	SFP+ (10GBA SE-R) (Crimson) / qSFP+ (Cyan)		
Management interface (see Note 1)	RJ45		
MTBF (see Note 3)	23.6k hrs @ 40degC		
Volume (See Note 4)	19 inch server rack: 1U (Crimson) / 3U (Cyan)		
Mass	8kg (Crimson) / 11kg (Cyan)		
# of receive channels	0-16		
# of transmit channels	0-16		
Receive instantaneous bandwidth at FPGA	Up to 1GHz per channel		
Transmit instantaneous bandwidth at FPGA	Up to 1GHz per channel		
ADC resolution	16 bit		
DAC resolution	16 bit		
ADC sampling rate	up to 320MSPS (Crimson) / up to 1GSPS (Cyan)		
DAC sampling rate	up to 320MSPS (Crimson) / up to 1GSPS (Cyan)		
Frequency resolution	0.0625 Hz		
Frequency accuracy	2ppm (Crimson) / 50 ppb (Cyan)		
Adjustable pulse width	Available		
Real time kernal option	Available		

Note 1: This parameter may be adjusted to customer requirements.
Note 2: Product supports fast tuning times between frequencies that are integer multiples of one other. Arbitrary frequencies may take longer.
Note 3: Mean time between failure is calculated assuming sustained operation at environmental limits, and includes any single source of failures, including fans.
Note 4: The form factor may be optimized to accommodate SWaP requirements.
Note 5: Minimum Demod SNR is based on specific BER. SNR may be adjusted to accommodate different BER specifications.
Note 6: Total latency measured relative to speed of light, and assumes 1 byte transmission, with 10 ^-5 BER.

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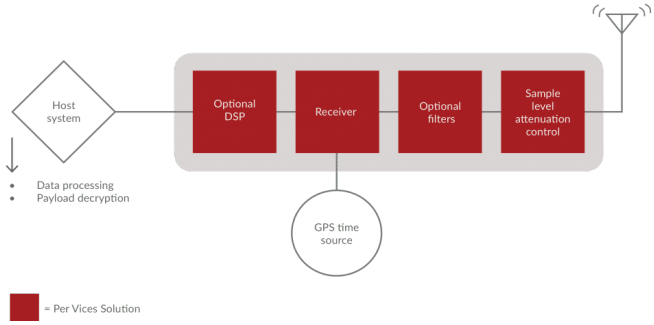
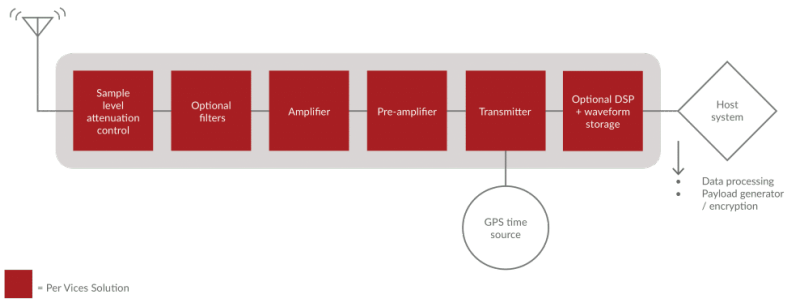
LOW LATENCY BLOCK DIAGRAM RX



LOW LATENCY BLOCK DIAGRAM TX



INTERNAL ARCHITECTURE

The figures above show a typical network with different locations for the transmit (Tx) and receive (Rx) equipment. Network packets, containing a payload are transmitted from one endpoint and received at the other. SDRs reduce latencies experienced on both the Tx and Rx sides of the system.

In addition to managing communications with the host computer, the FPGA supports on-board storage and in-unit DSP capabilities for quick responses. Both ends of the system have an amplifier, filters, and attenuation controls that are applied to analog signals directly. On the Rx chain, the ADC samples the incoming wave at up to 320 MSPS on Crimson, and up to 1 GSPS on Cyan. The high-sampling frequency allows the system to capture more data-points for processing later on.

INTEGRATION CAPABILITIES
API Documentation
Antenna Interface
Data Interface
Management Interface
FPGA Logic Elements
TFLOPS
Volume
Mass

SDR INTEGRATION

Per Vices SDRs provide high precision timing for systems through network or GPS interfaces. System complexity can be easily managed through common SDR software tools, while still being able to offload the computationally intensive DSP portions to the FPGA. The radio may be configured for user SWaP requirements. Our radios are built for 19 inch server racks, with a 10GBase-R or 40GBase-R data interfaces, and a RJ45 Management interface, making them easily adaptable for new or existing systems.

PRODUCTION CAPABILITIES

Get started quickly with our COTS solutions, before proceeding to fully integrated solutions. Guaranteed performance with standard factory test reports and customer specified reports. Per Vices scales low, medium, and high volume capabilities to match the size of your project.

EVALUATION REQUIREMENTS

Get started quickly with our COTS modem solutions, where we recommend working with the units in a lab environment as a proof of concept (POC). This helps reduce risk and can simulate the expected performance as it relates to reliability and latency. We can also work with you to do initial link establishment between your receive and transmit locations.

CONTACT US

More information is available at www.pervices.com.
If you have any questions, please contact us at solutions@pervices.com.